UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,551	09/26/2003	Seiji Funaba	17072	3724

23389 7590 12/28/2005

SCULLY SCOTT MURPHY & PRESSER, PC
400 GARDEN CITY PLAZA
SUITE 300
GARDEN CITY, NY 11530

EXAMINER	
SANDVIK, BENJAMIN P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,551	FUNABA ET AL.	
	Examiner	Art Unit	
	Ben P. Sandvik	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *24 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-73* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13,14,17,19,23,25,31 and 35* is/are allowed.

6)☒ Claim(s) *1,2,5,7,55,60,61 and 68* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1, 2, 5, 7, 11, 13, 14, 17, 19, 23, 25, 31, 35, 55, 60, 61, 68, 72 in the reply filed on 10/24/2005 is acknowledged.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5, 55, 60, 61, and 68 are rejected under 35 U.S.C. 103(a) as being anticipated by Funaba et al (U.S. PG Pub #2001/0022739), in view of Devnani et al (U.S. Patent #6630628).

With respect to **claim 1**, Funaba teaches a laminated substrate comprising at least two wiring layers which include a signal wiring layer (Fig. 52, 107) and a power/supply or ground wiring layer (Fig. 52, 108 and 109), said laminated substrate having a main surface; and a semiconductor chip (Fig. 52, 11), said two device terminals (Fig. 50, solder balls) being mounted on said laminated substrate and being connected to both ends of a signal wire in said signal wiring layer, said signal wire being connected to the input/output pad of said semiconductor chip through a via hole (Fig. 50, each chip 11 has two vias

extending from the signal layer to corresponding solder balls or "device terminals"). Funaba does not teach the semiconductor chip having an input/output pad and being mounted on the main surface of said laminated substrate through said input/output pad. Devnani teaches input/output pads on a chip being used to mount the chip on a substrate (Col 3 Ln 35, "metalized pads). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide metalized pads on the chip of Funaba as taught by Devnani in order to facilitate an electrical connection to the solder balls.

With respect to **claim 5**, Funaba and Devnani teach all of the limitations of claim 1, but Funaba does not teach that the signal wiring layer forms a micro-strip line with the ground wiring layer in said laminated substrate, said ground wiring layer being disposed between said signal wiring layer and said semiconductor chip. Devnani teaches that the signal layer forms a micro strip line and that the ground wiring layer (Fig. 2, 140) is disposed between the signal layer (Fig. 2, 150) and the semiconductor chip (Fig. 2, 105). It would have been obvious to one of ordinary skill in the art at the time the invention was made to arranged the signal and ground layers of Funaba as taught Devnani in order to optimize the wiring arrangement of the substrate.

With respect to **claim 55**, Funaba teaches a semiconductor unit having said two device terminals disposed in different sides of inside and outside of said

semiconductor unit one by one (Fig. 50, inside solder ball and outside solder ball of right chip 11), but does not teach that said two device terminals are wired to an input/output pad of a semiconductor chip. Devnani teaches solder balls that are wired to input/output pads of a chip (Col 3 Ln 35, "metalized pads). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide metalized pads on the chip of Funaba as taught by Devnani in order to facilitate an electrical connection to the solder balls.

With respect to **claim 60**, Funaba teaches a laminated substrate comprising at least two wiring layers including a signal wiring layer (Fig. 52, 107) and a power-supply or a ground wiring layer (Fig. 52, 108 and 109), said laminated substrate having a main surface and a back surface; and a semiconductor chip (Fig. 52, 11), said semiconductor chip being mounted on the main surface of said laminated substrate, said two device terminals being disposed on the main surface and the back surface of said laminated substrate opposite to each other (Fig. 50, solder balls), respectively, said two device terminals being connected to each other through a via hole (Fig. 52, the outside solder balls of chips 11 are connected to the outside solder balls of the opposite chip by means of a via), but Funaba does not teach the semiconductor chip having an input/output pad, or said via hole being connected to the semiconductor chip through a wire. Devnani teaches solder balls that are wired to input/output pads of a chip (Col 3 Ln 35, "metalized pads). It would have been obvious to one of ordinary skill in the art at the time the invention was made to

provide metalized pads on the chip of Funaba as taught by Devnani in order to facilitate an electrical connection to the solder balls. Devnani also teaches a via (Fig. 2, 160) being connected to a semiconductor chip through a wire (Fig. 2, 155). It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the via of Funaba to the semiconductor chip with a wire as taught by Devnani in order to have greater flexibility in wiring than with a sole solder ball.

With respect to **claim 61**, Funaba teaches a laminated substrate comprising at least two wiring layers including a signal wiring layer (Fig. 52, 107) and a power-supply or a ground wiring layer (Fig. 52, 108 and 109), said laminated substrate having a main surface and a back surface; and two semiconductor chips, said semiconductor chips being mounted on the main surface and the back surface of said laminated substrate (Fig. 52, 11), respectively, said two device terminals being disposed on the main surface and the back surface of said laminated substrate opposite to each other, respectively, said two device terminals being connected to each other through a via hole (Fig. 52, the outside solder balls of chips 11 are connected to the outside solder balls of the opposite chip by means of a via), but Funaba does not teach the semiconductor chip having an input/output pad, or said via hole being connected to the semiconductor chip through a wire. Devnani teaches solder balls that are wired to input/output pads of a chip (Col 3 Ln 35, "metalized pads). It would have been obvious to one of ordinary skill in the art at the time the invention was made

to provide metalized pads on the chip of Funaba as taught by Devnani in order to facilitate an electrical connection to the solder balls. Devnani also teaches a via (Fig. 2, 160) being connected to a semiconductor chip through a wire (Fig. 2, 155). It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the via of Funaba to the semiconductor chip with a wire as taught by Devnani in order to have greater flexibility in wiring than with a sole solder ball.

With respect to **claim 68**, Funaba teaches that said semiconductor unit further has different four device terminals every at least one signal (Fig. 40A, top and bottom outer solder balls), first and second terminals in said different four device terminals being disposed on the main and the back surfaces of said laminated substrate at left side opposite to each other (Fig. 40A, rightmost two solder balls on top and bottom of substrate), third and fourth terminals of said different four device terminals being disposed on the main and the back surfaces of said laminated substrate at right side opposite to each other (Fig. 40A, leftmost two solder balls on top and bottom of substrate), said first and said second terminals and said third and said fourth terminals being disposed at left and right of said laminated substrate opposite to each other, said first and said second terminals being connected to each other through a first via hole (Fig. 40B, top via hole 200), said third and said fourth terminals being connected to each other through a second via hole (Fig. 40B, bottom via hole 200), said first and said

second via holes being connected to a corresponding signal pad of said semiconductor chip by a wire, respectively (Fig. 40A, 15).

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Funaba and Devnani, in view of Yew et al (U.S. Patent #6137164).

With respect to **claim 2**, Funaba and Devnani teach all of the limitations of claim 1, but do not teach that the semiconductor chip comprises a circuit comprising at least one of an input buffer and an output buffer, an input protection resistor, and an electrostatic protection element. Yew teaches a chip having a layer of polymeric chip coating material (Col 6 Ln 39-41). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a layer of polymeric chip coating material to the chip of Funaba as taught by Yew in order to give the chip electrostatic protection.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Funaba and Devnani, in view of Tanahashi (U.S. Patent #6184477).

With respect to **claim 7**, Funaba and Devnani teach all of the limitations of claim 1, but do not teach said signal wiring layer being sandwiched between the power-supply layer and the ground layer in said laminated substrate, said signal wiring layer forming a strip line with the power-supply layer or the ground layer. Tanahashi teaches a signal layer (Fig. 6, S1) between a power layer (Fig. 6, P) and a ground layer (Fig. 6, G), the signal layer forming a strip line (Fig. 5, S1). It

would have been obvious to one of ordinary skill in the art at the time the invention was made to arranged the wiring layers of Funaba as taught by Tanahashi in order to optimize the electrical characteristics of the device.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 72 rejected under 35 U.S.C. 102(b) as being anticipated by Funaba.

With respect to **claim 72**, Funaba teaches a package having a main surface and a back surface, said package having at least two ball terminal adhesive areas every one input/output signal on the main and the back surfaces of said package, a ball terminal being adhered to only one ball terminal adhesive area on one surface of said package (Fig. 38A/B, each solder is attached to only one solder ball terminal adhesive area).

Allowable Subject Matter

Claims 13, 14, 17, 19, 23, 25, 31, 35 allowed.

Claim 11 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

bps